

ABSTRACT

An apparatus for determining the validity of a data signal communicated between two microprocessors by a dual port random access memory (RAM). The apparatus includes a sender for providing a data signal and an initialization status indicator, and a dual port RAM in communication with the sender for receiving the data signal and the initialization status indicator. The dual port RAM has a first memory location for storing the data signal and a second memory location for storing the initialization status indicator of the dual port RAM. The sender performs initialization on the dual port RAM at the beginning of a data transfer cycle which includes a plurality of data transfer from the sender to a receiver. The sender updates the initialization status indicator as the initialization progresses. The receiver of the apparatus is in communication with the dual port RAM. More particularly, the receiver reads the initialization status of the dual port RAM from the second memory location. The receiver subsequently reads the data signal from the first memory location in association with the operation status of the dual port RAM.